IN THE CLAIMS

1. (Currently Amended) A system for providing parallel processing of data to a plurality of digital signal processors (DSPs), comprising:

means for transmitting communication data to a load management system from at least one CPU, wherein the load management system includes:

a plurality of direct memory access (DMA) devices, each DMA device having one or more internal registers, one or more FIFOs, and a state machine associated with the one or more FIFOs;

a memory interface for interfacing the plurality of DMA devices with an external memory device;

a plurality of status and control registers coupled to the plurality of DMA devices;

at least one CPU interface for interfacing the at least one CPU with the plurality of status and control registers; and

a plurality of DSP interfaces for interfacing the plurality of DSPs with the plurality of DMA devices, wherein each of the plurality of DSP interfaces includes a program/data memory and a ping pong memory;

an external memory, wherein the external memory is coupled to the plurality of DSPs through a plurality of dedicated memory threads;

means for selecting two or more DSPs from the plurality of DSPs for processing the communication data using the load management system;

means for processing the communication data using the selected two or more DSPs and the load management system; and

means for transmitting the processed communication data back to the at least one CPU and to a communication device, wherein the at least one CPU interface includes at least one routing MUX, wherein the at least one routing MUX is coupled to the external memory device.

2. (Previously presented) The system of claim 1, wherein the communication data is transmitted from a VoIP system.

3. (Previously presented) The system of claim 1, wherein the communication data is transmitted from a FoP system.

4. (Previously presented) The system of claim 1, wherein the communication data is transmitted from an IP to sonet system.

5. (Previously presented) The system of claim 1, wherein the communication data is transmitted from an encoder/decoder.

6. (Previously presented) The system of claim 1, wherein the communication data is transmitted from a broadband communication system.

7. (Previously presented) The system of claim 1, wherein the communication data is transmitted from an image processing system.

8. (Previously presented) The system of claim 1, wherein the communication data is transmitted from a data modem.

9-12. (Canceled).

13. (Currently Amended) The system of claim 1 ~~12~~, wherein the external memory device comprises a memory access controller array.

14. (Currently Amended) The system of claim 1 ~~12~~, wherein the external memory device comprises a memory management system.

15-32. (Canceled).

33. (Currently Amended) A method for providing parallel processing of data to a plurality of digital signal processors (DSPs), comprising the steps of:

transmitting communication data to a load management system from at least one CPU, wherein the load management system includes:

a plurality of direct memory access (DMA) devices, each DMA device having one or more internal registers, one or more FIFOs, and a state machine associated with the one or more FIFOs;

a memory interface for interfacing the plurality of DMA devices with an external memory device;

a plurality of status and control registers coupled to the plurality of DMA devices;

at least one CPU interface for interfacing the at least one CPU with the plurality of status and control registers; and

a plurality of DSP interfaces for interfacing the plurality of DSPs with the plurality of DMA devices, wherein each of the plurality of DSP interfaces includes a program/data memory and a ping pong memory;

coupling an external memory to the plurality of DSPs through a plurality of dedicated memory threads;

selecting two or more DSPs from the plurality of DSPs for processing the communication data using the load management system;

processing the communication data using the selected two or more DSPs and the load management system; and

transmitting the processed communication data back to the at least one CPU and to a communication device, wherein the at least one CPU interface includes at least one routing MUX, wherein the at least one routing MUX is coupled to the external memory device.